

HT1380

Features

- Operating voltage: 2.0V~5.5V
- Maximum input serial clock: 500kHz at $V_{DD}=2V$, 2MHz at $V_{DD}=5V$
- Operating current: less than $1\mu A$ at 2V, less than $1.2\mu A$ at 5V
- TTL compatible
 - V_{IH} : 2.0V~ $V_{DD}+0.3V$ at $V_{DD}=5V$
 - V_{IL} : $-0.3V\sim+0.8V$ at $V_{DD}=5V$
- Two data transmission modes: single-byte, or burst mode
- Serial I/O transmission
- All registers store BCD format
- HT1380: 8-pin DIP package
HT1381: 8-pin SOP package

Applications

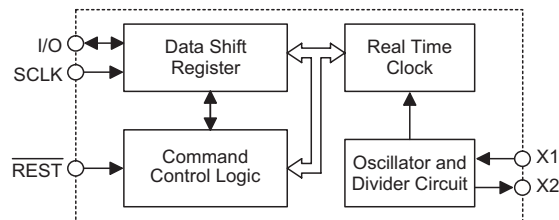
- Microcomputer serial clock
- Clock and Calendar

General Description

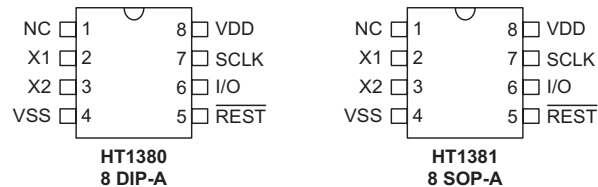
The HT1380/HT1381 is a serial timekeeper IC which provides seconds, minutes, hours, day, date, month and year information. The number of days in each month and leap years are automatically adjusted. The HT1380/HT1381 is designed for low power consumption and can operate in two modes: one is the 12-hour mode with an AM/PM indicator, the other is the 24-hour mode.

The HT1380/HT1381 has several registers to store the corresponding information with 8-bit data format. A 32768Hz crystal is required to provide the correct timing. In order to minimize the pin number, the HT1380/HT1381 use a serial I/O transmission method to interface with a microprocessor. Only three wires are required: (1) \overline{REST} , (2) SCLK and (3) I/O. Data can be delivered 1 byte at a time or in a burst of up to 8 bytes.

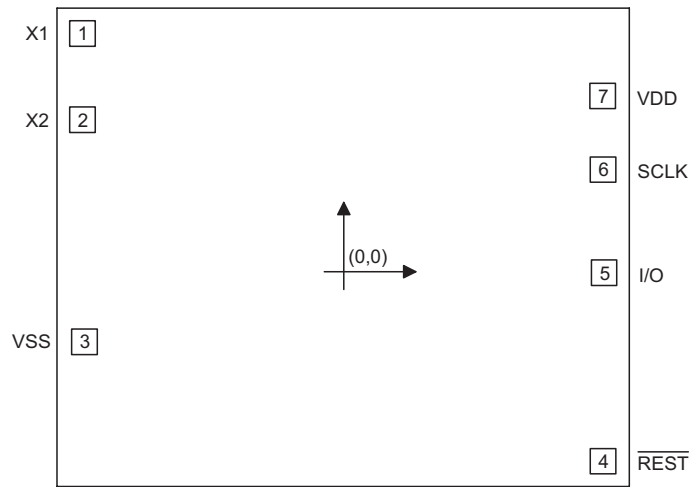
Block Diagram



Pin Assignment



Pad Assignment



Chip size: 2010 × 1920 (μm)²

* The IC substrate should be connected to VSS in the PCB layout artwork.

Pad Coordinates

Unit: μm

| Pad No. | X | Y |
|---------|---------|---------|
| 1 | -851.40 | 775.00 |
| 2 | -851.40 | 494.60 |
| 3 | -844.40 | -203.90 |
| 4 | 845.90 | -618.30 |
| 5 | 848.40 | -4.30 |
| 6 | 845.90 | 332.60 |
| 7 | 844.40 | 572.60 |

Pad Description

| Pad No. | Pad Name | I/O | Internal Connection | Description |
|---------|--------------------------|-----|---------------------|---|
| 1 | X1 | I | CMOS | 32768Hz crystal input pad |
| 2 | X2 | O | CMOS | Oscillator output pad |
| 3 | VSS | — | CMOS | Negative power supply, ground |
| 4 | $\overline{\text{REST}}$ | I | CMOS | Reset pin with serial transmission |
| 5 | I/O | I/O | CMOS | Data input/output pin with serial transmission |
| 6 | SCLK | I | CMOS | Serial clock pulse pin with serial transmission |
| 7 | VDD | — | CMOS | Positive power supply |

Absolute Maximum Ratings

| | | | |
|----------------------|--------------------------------|-----------------------------|----------------|
| Supply Voltage | -0.3V to 5.5V | Storage Temperature | -50°C to 125°C |
| Input Voltage | $V_{SS}-0.3V$ to $V_{DD}+0.3V$ | Operating Temperature | 0°C to 70°C |

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25°C

| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|-------------------|-------------------|-----------------|-----------------------|------|-------|------|------|
| | | V _{DD} | Conditions | | | | |
| V _{DD} | Operating Voltage | — | — | 2 | — | 5.5 | V |
| I _{STB} | Standby Current | 2V | — | — | — | 100 | nA |
| | | 5V | | — | — | 100 | nA |
| I _{DD} | Operating Current | 2V | No load | — | 0.7 | 1.0 | μA |
| | | 5V | | — | 0.7 | 1.2 | μA |
| I _{OH} | Source Current | 2V | V _{OH} =1.8V | -0.2 | -0.4 | — | mA |
| | | 5V | V _{OH} =4.5V | -0.5 | -1.0 | — | mA |
| I _{OL} | Sink Current | 2V | V _{OL} =0.2V | 0.7 | 1.5 | — | mA |
| | | 5V | V _{OL} =0.5V | 2.0 | 4.0 | — | mA |
| V _{IH} | "H" Input Voltage | 5V | — | 2 | — | — | V |
| V _{IL} | "L" Input Voltage | 5V | — | — | — | 0.8 | V |
| f _{OSC} | System Frequency | 5V | 32768Hz X'TAL | — | 32768 | — | Hz |
| f _{SCLK} | Serial Clock | 2V | — | — | — | 0.5 | MHz |
| | | 5V | | — | — | — | 2 |

Note: * I_{STB} is specified with SCLK, I/O, $\overline{\text{REST}}$ open. The clock halt bit must be set to logic 1 (oscillator disabled).

A.C. Characteristics

Ta=25°C

| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|------------------|---------------------|-----------------|------------|------|------|------|------|
| | | V _{DD} | Conditions | | | | |
| t _{DC} | Data to Clock Setup | 2V | — | 200 | — | — | ns |
| | | 5V | — | 50 | — | — | |
| t _{CDH} | Clock to Data Hold | 2V | — | 280 | — | — | ns |
| | | 5V | — | 70 | — | — | |
| t _{CDD} | Clock to Data Delay | 2V | — | — | — | 800 | ns |
| | | 5V | — | — | — | 200 | |
| t _{CL} | Clock Low Time | 2V | — | 1000 | — | — | ns |
| | | 5V | — | 250 | — | — | |
| t _{CH} | Clock High Time | 2V | — | 1000 | — | — | ns |
| | | 5V | — | 250 | — | — | |
| f _{CLK} | Clock Frequency | 2V | — | — | — | 0.5 | MHz |
| | | 5V | — | D.C. | — | 2.0 | |

| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|------------------|-----------------------------|-----------------|------------|------|------|------|------|
| | | V _{DD} | Conditions | | | | |
| t _r | Clock Rise and Fall Time | 2V | — | — | | 2000 | ns |
| t _f | | 5V | — | — | | 500 | |
| t _{CC} | Reset to Clock Setup | 2V | — | 4 | | — | us |
| | | 5V | — | 1 | | — | |
| t _{CCH} | Clock to Reset Hold | 2V | — | 240 | | — | ns |
| | | 5V | — | 60 | | — | |
| t _{CWH} | Reset Inactive Time | 2V | — | 4 | | — | us |
| | | 5V | — | 1 | | — | |
| t _{CDZ} | Reset to I/O High Impedance | 2V | — | — | | 280 | ns |
| | | 5V | — | — | | 70 | |

Functional Description

The HT1380/HT1381 mainly contains the following internal elements: a data shift register array to store the clock/calendar data, command control logic, oscillator circuit and read timer clock. The clock is contained in eight read/write registers as shown below. Data contained in the clock register is in binary coded decimal format.

Two modes are available for transferring the data between the microprocessor and the HT1380/HT1381. One is in single-byte mode and the other is in multiple-byte mode.

The HT1380/HT1381 also contains two additional bits, the clock halt bit (CH) and the write protect bit (WP).

These bits control the operation of the oscillator and so data can be written to the register array. These two bits should first be specified in order to read from and write to the register array properly.

Command Byte

For each data transfer, a Command Byte is initiated to specify which register is accessed. This is to determine whether a read, write, or test cycle is operated and whether a single byte or burst mode transfer is to occur. Refer to the table shown below and follow the steps to write the data to the chip. First give a Command Byte of HT1380/HT1381, and then write a data in the register.

This table illustrates the correlation between Command Byte and their bits:

| Function Description | Command Byte | | | | | | | |
|-------------------------------------|--------------|----|----|----|----|----|----|-----|
| | C7 | C6 | C5 | C4 | C3 | C2 | C1 | C0 |
| Select Read or Write Cycle | | | | | | | | R/W |
| Specify the Register to be Accessed | | | | | A2 | A1 | A0 | |
| Clock Halt Flag | C | | | | | | | |
| For IC Test Only | 1 | 0 | 0 | 1 | x | x | x | 1 |
| Select Single Byte or Burst Mode | 1 | 0 | 1 | 1 | 1 | 1 | 1 | x |

Note: "x" stands for don't care

The following table shows the register address and its data format:

| Register Name | Range Data | Register Definition | | | | | | | | Address A2~A0 | Bit R/W | Command Byte |
|---------------|----------------|---------------------|-------------|----------|----------|-------|----|-----|--------|----------------------|----------------------|--------------|
| | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | | |
| Seconds | 00~59 | CH | 10 SEC | | | SEC | | | 000 | W R | 10000000 10000001 | |
| Minutes | 00~59 | 0 | 10 MIN | | | MIN | | | 001 | W R | 10000010 10000011 | |
| Hours | 01~12 00~23 | 12\ 24 | 0 0 | AP 10 | HR HR | HOUR | | | 010 | W R | 10000100 10000101 | |
| Date | 01~31 | 0 | 0 | 10 DATE | | DATE | | | 011 | W R | 10000110 10000111 | |
| Month | 01~12 | 0 | 0 | 0 | 10M | MONTH | | | 100 | W R | 10001000 10001001 | |
| Day | 01~07 | 0 | 0 | 0 | 0 | DAY | | | 101 | W R | 10001010 10001011 | |
| Year | 00~99 | 10 YEAR | | | YEAR | | | 110 | W R | 10001100 10001101 | | |
| Write Protect | 00~80 | WP | ALWAYS ZERO | | | | | | 111 | W R | 10001110 10001111 | |

CH: Clock Halt bit

CH=0 oscillator enabled

CH=1 oscillator disabled

WP: Write protect bit

WP=0 register data can be written in

WP=1 register data can not be written in

Bit 7 of Reg2: 12/24 mode flag

bit 7=1, 12-hour mode

bit 7=0, 24-hour mode

Bit 5 of Reg2: AM/PM mode defined

AP=1 PM mode

AP=0 AM mode

R/W Signal

The LSB of the Command Byte determines whether the data in the register be read or be written to.

When it is set as "0" means that a write cycle is to take place otherwise this chip will be set into the read mode.

A0~A2

A0 to A2 of the Command Byte is used to specify which registers are to be accessed. There are eight registers used to control the month data, etc., and each of these registers have to be set as a write cycle in the initial time.

Burst Mode

When the Command Byte is 10111110 (or 10111111), the HT1380/HT1381 is configured in burst mode. In this mode the eight clock/calendar registers can be written (or read) in series, starting with bit 0 of register address 0 (see the timing on the next page).

Test Mode

When the Command Byte is set as 1001xxx1, HT1380/HT1381 is configured in test mode. The test mode is used by Holtek only for testing purposes. If used generally, unpredictable conditions may occur.

Write Protect Register

This register is used to prevent a write operation to any other register. Data can be written into the designated register only if the Write Protect signal (WP) is set to logic 0. The Write Protect Register should be set first before restarting the system or before writing the new data to the system, and it should set as logic 1 in the read cycle. The Write Protect bit cannot be written to in the burst mode.

Clock HALT Bit

D7 of the Seconds Register is defined as the Clock Halt Flag (CH).

When this bit is set to logic 1, the clock oscillator is stopped and the chip goes into a low-power standby mode. When this bit is written to logic 0, the clock will start.

12-hour/24-hour Mode

The D7 of the hour register is defined as the 12-hour or 24-hour mode select bit.

When this bit is in high level, the 12-hour mode is selected otherwise it's the 24-hour mode.

AM-PM Mode

These are two functions for the D5 of the hour register determined by the value D7 of the same register.

One is used in AM/PM selection on the 12-hour mode. When D5 is logic 1, it is PM, otherwise it's AM. The other is used to set the second 10-hour bit (20~23 hours) on the 24-hour mode.

Reset and Serial Clock Control

The $\overline{\text{REST}}$ pin is used to allow access data to the shift register like a toggle switch. When the $\overline{\text{REST}}$ pin is taken high, the built-in control logic is turned on and the address/command sequence can access the corresponding shift register. The REST pin is also used to terminate either single-byte or burst mode data format.

The input signal of SCLK is a sequence of a falling edge followed by a rising edge and it is used to synchronize the register data whether read or write. For data input, the data must be read after the rising edge of SCLK. The data on the I/O pin becomes output mode after the falling edge of the SCLK. All data transfer terminates if the $\overline{\text{REST}}$ pin is low and the I/O pin goes to a high impedance state. The data transfer is illustrated on the next page.

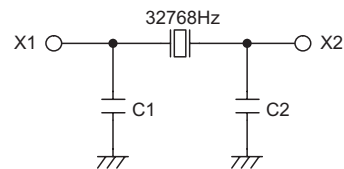
Data Input and Data Out

In writing a data byte with HT1380/HT1381, the read/write should first set as R/W=0 in the Command Byte and follow with the corresponding data register on the rising edge of the next eight SCLK cycles. Additional SCLK cycles are ignored. Data inputs are entered starting with bit 0.

In reading a data on the register of HT1380/HT1381, R/W=1 should first be entered as input. The data bit outputs on the falling edge of the next eight SCLK cycles. Note that the first data bit to be transmitted on the first falling edge after the last bit of the read command byte is written. Additional SCLK cycles re-transmits the data bytes as long as $\overline{\text{REST}}$ remains at high level. Data outputs are read starting with bit 0.

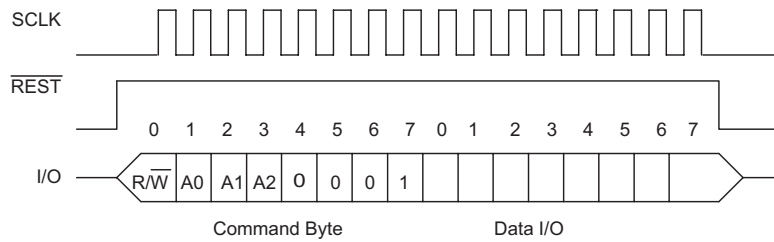
Crystal Selection

A 32768Hz crystal can be directly connected to the HT1380/HT1381 via pin 2 and pin 3 (X1, X2). In order to obtain the correct frequency, two additional load capacities (C1, C2) are needed. The value of the capacity depends on how accurate the crystal is. We suggest that you can follow the table on the next page.

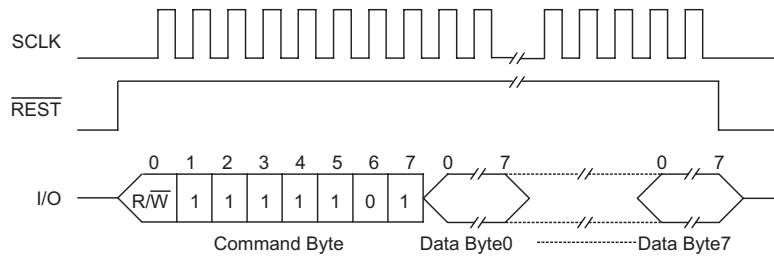


The following diagram shows the single and burst mode transfer:

• Single Byte Transfer



• Burst Mode Transfer



The table illustrates the values suggested for capacities C1, C2

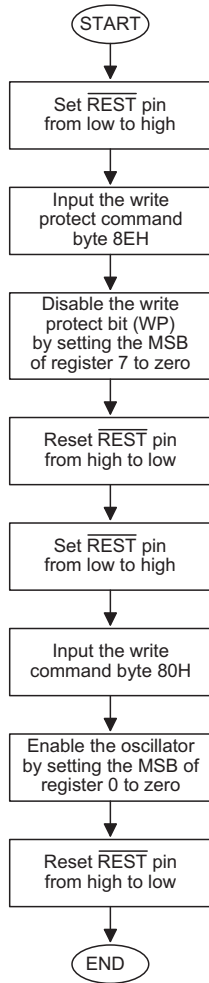
| Part No. | Crystal Error | Capacity Value |
|---------------|--------------------|----------------|
| HT1380/HT1381 | $\pm 10\text{ppm}$ | 5pF |
| | 10~20ppm | 8pF |

Operating Flowchart

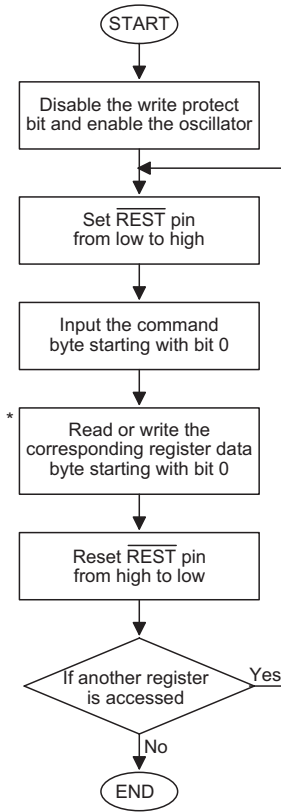
To initiate any transfer of data, $\overline{\text{REST}}$ is taken high and an 8-bit command byte is first loaded into the control logic to provide the register address and command information. Following the command word, the clock/calendar data is serially transferred to or from the corresponding register. The $\overline{\text{REST}}$ pin must be taken low again after the transfer operation is completed. All data enter on the rising edge of SCLK and outputs on the falling edge of SCLK. In total, 16 clock pulses are needed for a single byte mode and 72 for burst mode. Both input and output data starts with bit 0.

In using the HT1380/HT1381, set first the WP and CH to 0 and wait for about 3 seconds, the oscillator will generate the clocks for internal use. Then, choose either single mode or burst mode to input the data. The read or write operating flowcharts are shown on the next page.

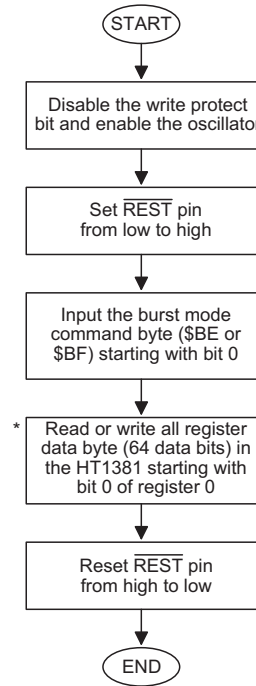
- To disable the write protect (WP=0) bit and enable the oscillator (CH=0)



- Single byte data transfer



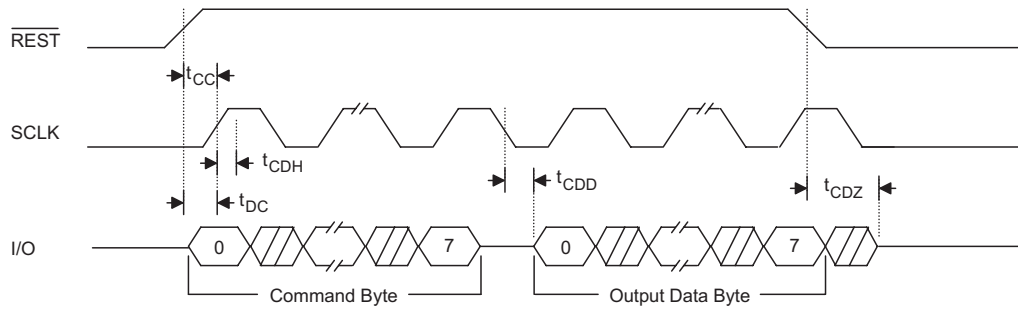
- Burst mode data transfer



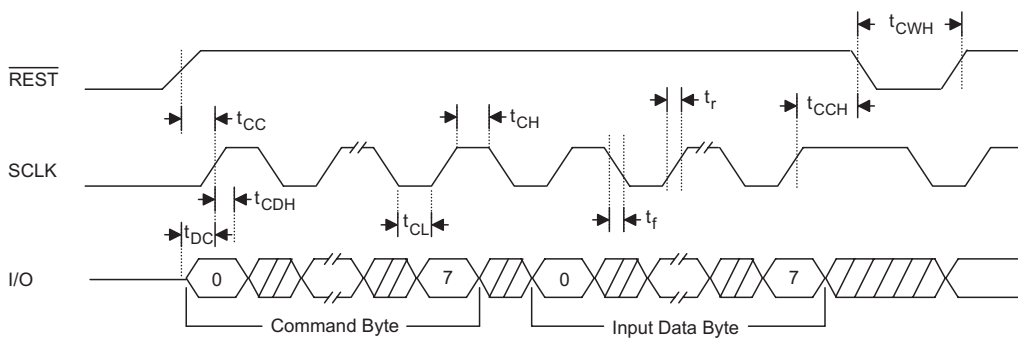
Note: * In reading data byte from HT1380/HT1381 register, the first data bit to be transmitted at the first falling edge after the last bit of the command byte is written.

Timing Diagrams

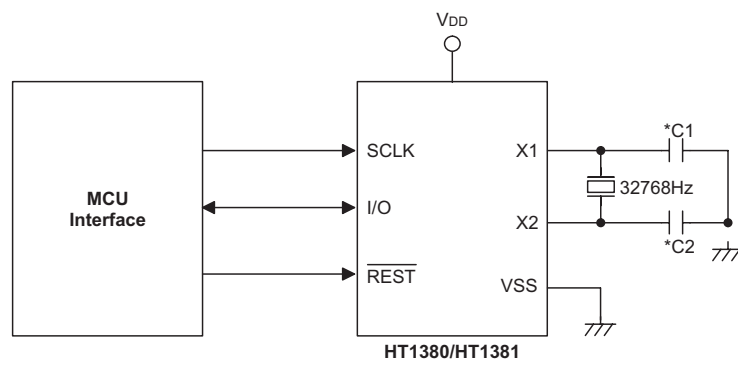
Read Data Transfer



Write Data Transfer



Application Circuits

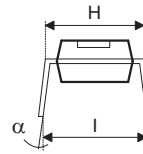
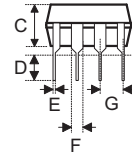
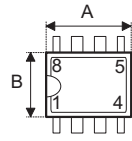


*Note: The value of the capacity depends on how accurate the crystal is.

Refer to the suggestion table of page 7.

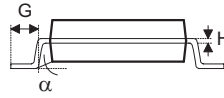
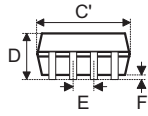
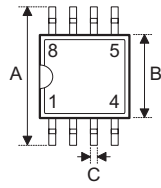
Package Information

8-pin DIP (300mil) Outline Dimensions



| Symbol | Dimensions in mil | | |
|----------|-------------------|------|------|
| | Min. | Nom. | Max. |
| A | 355 | — | 375 |
| B | 240 | — | 260 |
| C | 125 | — | 135 |
| D | 125 | — | 145 |
| E | 16 | — | 20 |
| F | 50 | — | 70 |
| G | — | 100 | — |
| H | 295 | — | 315 |
| I | 335 | — | 375 |
| α | 0° | — | 15° |

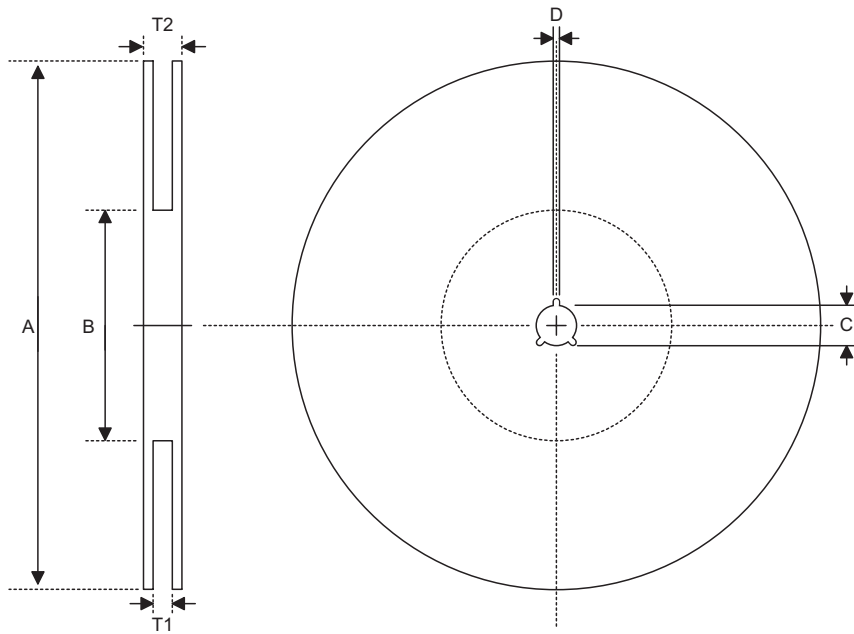
8-pin SOP (150mil) Outline Dimensions



| Symbol | Dimensions in mil | | |
|----------|-------------------|------|------|
| | Min. | Nom. | Max. |
| A | 228 | — | 244 |
| B | 149 | — | 157 |
| C | 14 | — | 20 |
| C' | 189 | — | 197 |
| D | 53 | — | 69 |
| E | — | 50 | — |
| F | 4 | — | 10 |
| G | 22 | — | 28 |
| H | 4 | — | 12 |
| α | 0° | — | 10° |

Product Tape and Reel Specifications

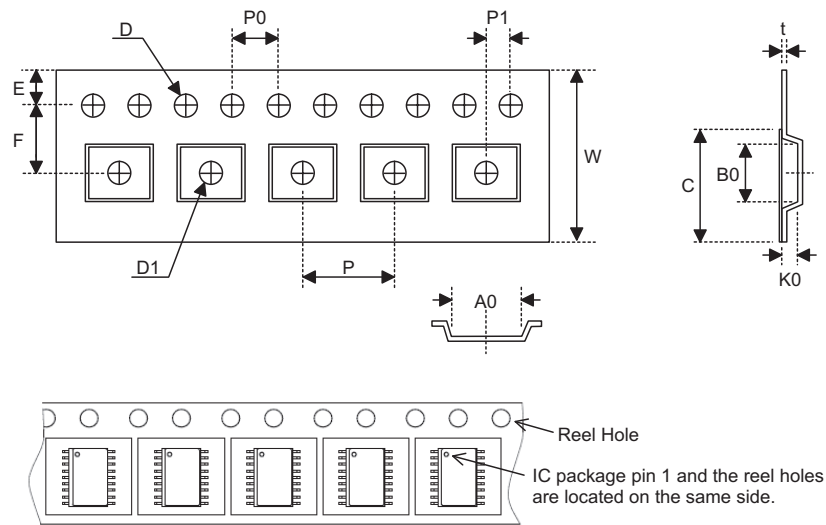
Reel Dimensions



SOP 8N

| Symbol | Description | Dimensions in mm |
|--------|-----------------------|------------------|
| A | Reel Outer Diameter | 330±1 |
| B | Reel Inner Diameter | 62±1.5 |
| C | Spindle Hole Diameter | 13+0.5 -0.2 |
| D | Key Slit Width | 2±0.5 |
| T1 | Space Between Flange | 12.8+0.3 -0.2 |
| T2 | Reel Thickness | 18.2±0.2 |

Carrier Tape Dimensions



SOP 8N

| Symbol | Description | Dimensions in mm |
|--------|--|--------------------|
| W | Carrier Tape Width | $12+0.3$ -0.1 |
| P | Cavity Pitch | 8 ± 0.1 |
| E | Perforation Position | 1.75 ± 0.1 |
| F | Cavity to Perforation (Width Direction) | 5.5 ± 0.1 |
| D | Perforation Diameter | 1.55 ± 0.1 |
| D1 | Cavity Hole Diameter | $1.5+0.25$ |
| P0 | Perforation Pitch | 4 ± 0.1 |
| P1 | Cavity to Perforation (Length Direction) | 2 ± 0.1 |
| A0 | Cavity Length | 6.4 ± 0.1 |
| B0 | Cavity Width | 5.2 ± 0.1 |
| K0 | Cavity Depth | 2.1 ± 0.1 |
| t | Carrier Tape Thickness | 0.3 ± 0.05 |
| C | Cover Tape Width | 9.3 |